

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Amended) A method for manufacturing a DRAM cell including two active word lines having a common drain/source region and having distinct source/drain regions contacting two memory points, comprising, after the forming of insulated conductive lines on a semiconductor substrate, the steps of:

- a) depositing a first insulating layer;
- b) depositing a second insulating layer, selectively etchable with respect to the first insulating layer;
- c) etching the second insulating layer to only maintain it above the insulated conductive lines, at least above an active region of the substrate;
- d) depositing and leveling a third thick insulating layer selectively etchable with respect to the second insulating layer;
- e) forming an opening in the first and third insulating layers to at least partially expose the common drain/source region and an insulating trench;
- f) depositing a conductive material to fill the previously-formed opening;
- g) performing a chem-mech polishing ~~of the entire structure~~; and
- h) depositing a fourth insulating layer, selectively etchable with respect to the third insulating layer.

2. (Original) The method of claim 1, wherein step e) consisting of forming the opening the first and third insulating layers to at least partially expose the common drain/source region and an insulating trench is implemented to open the first and third insulating layers to at least also partially expose the source/drain regions, and wherein the conductive material deposited at step f) is deposited to fill all the openings thus formed.

3. (Amended) The method of claim 1, wherein step e) consisting of opening the first and third insulating layers to at least partially expose the common drain/source regions and an insulating trench is preceded by the steps of:

- i) opening the first and third insulating layers to at least partially expose the source/drain regions;
- j) depositing a conductive material in the openings thus formed; and
- k) performing a chem-mech polishing ~~of the entire structure~~, whereby contacts are formed with the source/drain regions.

4. (Amended) The method of claim 3, wherein step k) of chem-mech polishing is followed by the deposition of an additional insulating layer ~~on the entire structure~~, step e) then consisting of successively opening the additional insulating layer and the first and third insulating layers to at least partially expose the common drain/source region and an insulating trench.

5. (Amended) The method of claim 1, wherein step g) of chem-mech polishing ~~of the entire structure~~, or step h) of deposition of the fourth insulating layer, selectively etchable with respect to the third insulating layer, is followed by the steps of:

- l) forming openings in said first and third insulating layers to at least partially expose the source/drain regions;
- m) depositing a conductive material in the openings thus formed; and
- n) performing a chem-mech polishing ~~of the entire structure~~, whereby contacts are formed with the source/drain regions.

6. (Original) The method of claim 1, wherein step a) of deposition of the first insulating layer is preceded by the deposition of an additional insulating layer selectively etchable with respect to a filling material of underlying insulating trenches and with respect to the first insulating layer.

7. (Original) The method of claim 6, wherein the first and third insulating layers are made of silicon oxide and wherein the second and fourth insulating layers as well as the additional insulating layer are made of silicon nitride.

8. (Original) The method of claim 1, wherein the memory cell is formed in a same substrate as logic circuits.

9-17. (Cancelled)

18. (Withdrawn) A method for manufacturing a DRAM cell structure, comprising:

forming insulating trenches on opposite sides of an active region of a substrate;

forming two inactive word lines on the insulating trenches;

forming two active word lines adjacent to opposite sides of a common drain/source region and adjacent to distinct source/drain regions contacting two memory points;

covering, at least partially, the four word lines, the insulating trenches, and the substrate with a multiple-layer having three insulating layers, formed of first and third layers deposited over the entire structure, and of a second layer removed from the active region, except above the word lines, and being made of a material selectively etchable with respect to the first and third layers;

forming an opening in the first and third insulating layers to expose the common drain-source region and one of the insulating trenches;

forming a bit line of the cell in the opening such that the bit line directly rests on the common drain/source region and on the exposed insulating trench;

covering the bit line and the third insulating layer being covered with a fourth insulating layer selectively etchable with respect to the third insulating layer.

19. (Withdrawn) The method of claim 18, wherein the multiple-layer is formed upon an additional insulating layer selectively etchable with respect to the first insulating layer and with respect to a filling material of the insulating trenches.

20. (Withdrawn) A method of manufacturing a memory device, comprising:
forming insulating trenches in a semiconductor substrate having an active region delineated by the insulating trenches;
forming first and second word lines on the substrate;
forming a common drain/source region in the active region between the first and second word lines;
forming source and drain regions positioned respectively in the active region on opposite sides of the first and second word lines with respect to the common drain/source region;
forming a plurality of insulating layers over the word lines, including a first insulating layer, a second insulating layer, removed from the active region except above the word lines, and a third insulating layer, the second insulating layer being selectively etchable with respect to the first and third insulating layers, the third insulating layer being leveled on an upper surface;
forming an opening in the first and third insulating layers above the common drain/source region and one of the insulating trenches;
forming a bit line of the memory device by filling the opening with a conductive material; and
forming a top insulating layer, selectively etchable with respect to the third insulating layer, above the third insulating layer and the bit line.

21. (Withdrawn) The method of claim 20, wherein the plurality of insulating layers includes a fourth insulating layer, selectively etchable with respect to the first insulating layer and a filling material of the insulating trenches, deposited between the semiconductor substrate and the first insulating layer.

22. (Withdrawn) The method of claim 20, further comprising:
forming additional openings in the second and third insulating layers above the source and drain regions; and
forming contacts by filling the additional openings with a conductive material.

23. (Withdrawn) The method of claim 20, wherein the conductive material of the bit line initially extends partially on the third insulating layer and the method further comprises removing the conductive material from the third insulating layer by etching until the bit line is substantially level with the upper surface of the third insulating layer.

24. ((Withdrawn) The method of claim 20, further comprising forming third and fourth word lines on the insulating trenches, wherein the first, second, and third insulating layers are formed above the third and fourth wordlines.

25. (Withdrawn) The method of claim 20, wherein the first and third insulating layers are made of silicon oxide and wherein the second and top insulating layers are made of silicon nitride.

26. (New) The method of claim 1 wherein step d) depositing and leveling the third insulating layer is performed after step c) etching the second insulating layer.

27. (New) The method of claim 26 wherein the third insulating layer contacts the first insulating layer through an opening formed in the second insulating layer above the active region during the etching step c).

28. (New) The method of claim 1 wherein step e) forming an opening comprises forming a channel in at least the third insulating layer above the insulating trench, and wherein step f) depositing the conductive material comprises filling the trench with conductive material to form a bit line.

29. (New) A method for manufacturing a DRAM cell, comprising:

- forming an insulating trench in a semiconductor substrate to define a boundary of an active region of the substrate;
- forming a wordline across the active region and insulated therefrom;
- depositing a first insulating layer over the substrate and wordline;
- depositing a second insulating layer, selectively etchable with respect to the first insulating layer, over the first insulating layer;
- etching a first opening in the second insulating layer above a portion of the active region of the substrate without exposing any portion of the first insulating layer directly above the wordline;
- depositing, after the etching step, a third insulating layer, selectively etchable with respect to the second insulating layer, over the first and second insulating layers and in the first opening;
- etching a second opening in the first and third insulating layers at the first opening; and
- depositing a conductive material within the second opening.

30. (New) The method of claim 29 wherein the etching the second opening step comprises etching a channel in at least the third insulating layer over the insulating trench, and wherein the depositing the conductive material step includes depositing conductive material in the channel.

31. (New) The method of claim 29, further comprising planarizing an upper surface of the third insulating layer.

32. (New) The method of claim 31 wherein the planarizing step is performed after the depositing conductive material step, and wherein the planarizing step comprises removing conductive material from above the upper surface of the third insulating layer.

33. (New) The method of claim 29 wherein the etching a second opening step comprises exposing a common drain/source region of the DRAM cell.

34. (New) The method of claim 29, further comprising etching a third opening in the first and third insulating layers at the first opening, and depositing a conductive material within the third opening.

35. (New) The method of claim 34 wherein the etching a third opening step is performed after the planarizing step.

36. (New) The method of claim 29, further comprising depositing a fourth insulating layer over the third insulating layer.

37. (New) The method of claim 29, further comprising depositing a fourth insulating layer prior to depositing the first insulating layer.